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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
SIDDIQUI, SAQIB JAVAID	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 08/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/709,238	SAHA ET AL.	
	Examiner	Art Unit	
	Saqib J. Siddiqui	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,5-7,10,12,14 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,5-7, 10, 12 & 14-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant's response was received and entered June 08, 2006.

- Claims 1, 5-7, 10, 12, & 14-15 are pending. Claims 1, 5-7, 10, 12 & 13 are amended.
- Claims 2-4, 8-9, 11 & 13 are canceled.
- Application is currently pending.

Response to Amendment

Applicant's arguments and amendments with respect to amended claims 1, 5-7, 10, 12, & 14-15 and previously presented claims 15 filed June 08, 2006 have been fully considered but they are not persuasive. The Examiner would like to point out that this action is made final (See MPEP 706.07a).

Applicant contends that the combination of the cited references does not teach scanning a second plurality of bits while the first plurality of tests are being performed. Applicant respectfully disagrees. Roohparvar mentions in claims 1 and 2 "means for altering execution of the memory erase operation during a test mode to bypass the erase step and programming the first memory cell using a test pattern input by a user.... **wherein the means for altering execution of the memory erase operation comprises: a test pattern data input circuit**; and a test pattern determiner operable to generate a second test pattern" (claims 1-2). Further Arimoto et al. teaches "In clock cycle #3, data Dout read from DRAM core MCR is temporarily stored in first-in first-out

circuit 10. Therefore, even if I/O pin terminal group 9 is externally supplied with test input data Din together with the test control signal forming write command WRITE in this clock cycle #3, conflict does not occur between the data read from DRAM core MCR and the test input data" (columns 9-10). Therefore clearly, more test patterns are being supplied while the testing is not complete. Further, examiner would like to point out that scanning a second plurality of bits is merely an iteration which involves routine skill in the art.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 5-7, 10, 12, & 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimoto et al. US Pat no. 6,404,684 B2 and further in view of Roohparvar US Pat no. 6,243,839 B1.

As per claim 1:

Arimoto et al. substantially teaches a method of testing an integrated circuit, said method comprising (Figure 1): scanning in a plurality of bits sequentially on a pin (Figure 1, "TD", column 8, lines 22-30), said plurality of bits forming a test code which indicates the test to be performed (column 11, lines 1-40); and performing said specific one of test in parallel (column 9, lines 1-50), wherein each of said plurality of bits indicates whether a corresponding one of test is to be performed (Figure 3, "Tdin", column 11, lines 1-10), further comprising: shifting in said plurality of bits into a shift register (Figure 3 # 20); and loading said plurality of bits from said shift register to a second register (Figure 3 # 21), wherein a bit value in each bit of said second register determines whether a corresponding one of said test is to be performed (column 11, lines 1-30), wherein said shifting and said performing are performed in parallel (Figure 3, column 11, lines 1-45). Using an output of the second register, performing specific ones of the first plurality of tests indicated by each one of the first plurality of bits and

scanning in a second plurality of bits sequentially on the pin into the first register while performing specific ones of the first plurality of tests, (columns 9-10) the second plurality of bits forming a second test code and each one of second plurality of bits represent a corresponding ones of a second plurality of test to be performed and further indicating whether the corresponding one of the second plurality of test is to be performed (claims 1-2).

Arimoto et al. does not explicitly teach performing a plurality of tests.

However Roohparvar in an analogous art teaches the method of parallel testing of memory cells performing a plurality of tests on the memory cells (column 5, lines 30-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the command decoder of Arimoto et al. to decode the plurality of bits into a plurality of tests after bit expansion, since one of ordinary skill in the art would have realized that enabling Arimoto et al.'s invention to have available a plurality of tests would allow for a more encompassing testing of the various DRAM memory cells and pages. This will benefit Arimoto et al.'s invention by giving the testing process the flexibility to perform a variety of tests so that the memory can be test for a variety of errors, which would not be possible with one testing procedure. It should be noted that Arimoto et al. explicitly mentions (column 17-18, lines 40-25) that this invention is not restricted to DRAM memory or does not have constraints on test patterns, hence it would have been obvious to one of ordinary skill in the art to incorporate a plurality if tests to allow for the testing of different types of memories. Further it should be noted that applying plurality of tests during parallel testing was

commonly known method in the testing of memories at the time the invention was made and it would have been obvious to one of ordinary skill in the art to apply this in Arimoto et al.'s invention.

As per claim 5:

Arimoto et al. substantially teaches a method of testing an integrated circuit, said method comprising (Figure 1): scanning in a plurality of bits sequentially on a pin (Figure 1, "TD", column 8, lines 22-30), said plurality of bits forming a test code which indicates the test to be performed (column 11, lines 1-40); and performing said specific one of test in parallel (column 9, lines 1-50), wherein each of said plurality of bits indicates whether a corresponding one of test is to be performed (Figure 3, "Tdin", column 11, lines 1-10), further comprising: shifting in said plurality of bits into a shift register (Figure 3 # 20); and loading said plurality of bits from said shift register to a second register (Figure 3 # 21), wherein a bit value in each bit of said second register determines whether a corresponding one of said test is to be performed (column 11, lines 1-30), wherein said shifting and said performing are performed in parallel (Figure 3, column 11, lines 1-45), wherein said scanning scans a plurality of control bits, said plurality of control bits representing control signals associated with said test (Figure 1 "TCMD").

Arimoto et al. does not explicitly teach performing a plurality of tests, wherein said scanning scans a plurality of control bits on said pin.

However Roohparvar in an analogous art teaches the method of parallel testing of memory cells performing a plurality of tests on the memory cells (column 5, lines 30-

65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the command decoder of Arimoto et al. to decode the plurality of bits into a plurality of tests after bit expansion, since one of ordinary skill in the art would have realized that enabling Arimoto et al.'s invention to have available a plurality of tests would allow for a more encompassing testing of the various DRAM memory cells and pages. This will benefit Arimoto et al.'s invention by giving the testing process the flexibility to perform a variety of tests so that the memory can be test for a variety of errors, which would not be possible with one testing procedure. It should be noted that Arimoto et al. explicitly mentions (column 17-18, lines 40-25) that this invention is not restricted to DRAM memory or does not have constraints on test patterns, hence it would have been obvious to one of ordinary skill in the art to incorporate a plurality if tests to allow for the testing of different types of memories. Further it should be noted that applying plurality of tests during parallel testing was commonly known method in the testing of memories at the time the invention was made and it would have been obvious to one of ordinary skill in the art to apply this in Arimoto et al.'s invention. It would be obvious to one of ordinary skill in the art at the time the invention was made to scan the control bits (Figure 3, "TCMD") on the same pin as the data input pins since the bits are both being input into Figure 1 # 1, since one or ordinary skill in the art would have realized that doing so would have allowed for further reducing the resources and hence making the testing more efficient. Further it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the same pin to input control bits and test input bits, since it has been held that

where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art. *In re Aller*,105 USPQ 233.

As per claim 6:

Arimoto et al. substantially teaches a method of testing an integrated circuit, said method comprising (Figure 1): scanning in a plurality of bits sequentially on a pin (Figure 1, "TD", column 8, lines 22-30), said plurality of bits forming a test code which indicates the test to be performed (column 11, lines 1-40); and performing said specific one of test in parallel (column 9, lines 1-50), wherein each of said plurality of bits indicates whether a corresponding one of test is to be performed (Figure 3, "Tdin", column 11, lines 1-10), further comprising: shifting in said plurality of bits into a shift register (Figure 3 # 20); and loading said plurality of bits from said shift register to a second register (Figure 3 # 21), wherein a bit value in each bit of said second register determines whether a corresponding one of said test is to be performed (column 11, lines 1-30), wherein said shifting and said performing are performed in parallel (Figure 3, column 11, lines 1-45), wherein said scanning scans a plurality of control bits, said plurality of control bits representing control signals associated with said plurality of tests (Figure 1 "TCMD"), wherein said scanning scans some bits of said test code on a first pin (Figure 1 "TD") and some other bits of said test code on a second pin (Figure 1 "TAD" is part of the test code), wherein said pin corresponds to one of said first pin and said second pin (column 11, lines 1-5).

Arimoto et al. does not explicitly teach performing a plurality of tests, wherein said scanning scans a plurality of control bits on said pin.

However Roohparvar in an analogous art teaches the method of parallel testing of memory cells performing a plurality of tests on the memory cells (column 5, lines 30-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the command decoder of Arimoto et al. to decode the plurality of bits into a plurality of tests after bit expansion, since one of ordinary skill in the art would have realized that enabling Arimoto et al.'s invention to have available a plurality of tests would allow for a more encompassing testing of the various DRAM memory cells and pages. This will benefit Arimoto et al.'s invention by giving the testing process the flexibility to perform a variety of tests so that the memory can be test for a variety of errors, which would not be possible with one testing procedure. It should be noted that Arimoto et al. explicitly mentions (column 17-18, lines 40-25) that this invention is not restricted to DRAM memory or does not have constraints on test patterns, hence it would have been obvious to one of ordinary skill in the art to incorporate a plurality if tests to allow for the testing of different types of memories. Further it should be noted that applying plurality of tests during parallel testing was commonly known method in the testing of memories at the time the invention was made and it would have been obvious to one of ordinary skill in the art to apply this in Arimoto et al.'s invention. It would be obvious to one of ordinary skill in the art at the time the invention was made to scan the control bits (Figure 3, "TCMD") on the same pin as the data input pins since the bits are both being input into Figure 1 # 1, since one or

ordinary skill in the art would have realized that doing so would have allowed for further reducing the resources and hence making the testing more efficient. Further it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the same pin to input control bits and test input bits, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art. *In re Aller*,105 USPQ 233.

As per claim 7:

Arimoto et al. substantially teaches a tests enabler block reducing a number of pins required to test an integrated circuit, said tests enabler block (Figure 1, "TIC") being contained in said integrated circuit (Figure 1), said tests enabler block comprising: a first pin receiving a plurality of bits sequentially (Figure 1, "TD"), said plurality of bits forming a test code which indicates the specific one of test to be performed to test said integrated circuit (column 11, lines 1-40), wherein the plurality of bits indicates whether a test is to be performed (column 9, lines 1-50), further comprising a first storage element storing said plurality of bits (column 8, lines 40-42), wherein a bit value in each bit of said first storage element determines whether a test is to be performed (column 8, lines 42-60, the "FIFO" is part of the "TIC", hence the FIFO indirectly determines whether a test is to be performed). Using an output of the second register, performing specific ones of the first plurality of tests indicated by each one of the first plurality of bits and scanning in a second plurality of bits sequentially on the pin into the first register while performing specific ones of the first plurality of tests, (columns 9-10) the

second plurality of bits forming a second test code and each one of second plurality of bits represent a corresponding ones of a second plurality of test to be performed and further indicating whether the corresponding one of the second plurality of test is to be performed (claims 1-2).

Arimoto et al. does not explicitly teach performing a plurality of tests.

However Roohparvar in an analogous art teaches the method of parallel testing of memory cells performing a plurality of tests on the memory cells (column 5, lines 30-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the command decoder of Arimoto et al. to decode the plurality of bits into a plurality of tests after bit expansion, since one of ordinary skill in the art would have realized that enabling Arimoto et al.'s invention to have available a plurality of tests would allow for a more encompassing testing of the various DRAM memory cells and pages. This will benefit Arimoto et al.'s invention by giving the testing process the flexibility to perform a variety of tests so that the memory can be test for a variety of errors, which would not be possible with one testing procedure. It should be noted that Arimoto et al. explicitly mentions (column 17-18, lines 40-25) that this invention is not restricted to DRAM memory or does not have constraints on test patterns, hence it would have been obvious to one of ordinary skill in the art to incorporate a plurality if tests to allow for the testing of different types of memories. Further it should be noted that applying plurality of tests during parallel testing was commonly known method in the testing of memories at the time the invention was made and it would have been obvious to one of ordinary skill in the art to apply this in Arimoto

et al.'s invention.

As per claim 10:

Arimoto et al. substantially teaches a tests enabler block reducing a number of pins required to test an integrated circuit, said tests enabler block (Figure 1, "TIC") being contained in said integrated circuit (Figure 1), said tests enabler block comprising: a first pin receiving a plurality of bits sequentially (Figure 1, "TD"), said plurality of bits forming a test code which indicates the specific one of test to be performed to test said integrated circuit (column 11, lines 1-40), wherein the plurality of bits indicates whether a test is to be performed (column 9, lines 1-50), further comprising a first storage element storing said plurality of bits (column 8, lines 40-42), wherein a bit value in each bit of said first storage element determines whether a test is to be performed (column 8, lines 42-60, the "FIFO" is part of the "TIC", hence the FIFO indirectly determines whether a test is to be performed), further comprises a shift register into which said plurality of bits are shifted in sequentially after being received by said first pin (Figure 1 # 1).

Arimoto et al. does not explicitly teach performing a plurality of tests.

However Roohparvar in an analogous art teaches the method of parallel testing of memory cells performing a plurality of tests on the memory cells (column 5, lines 30-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the command decoder of Arimoto et al. to decode the plurality of bits into a plurality of tests after bit expansion, since one of ordinary skill in the art would have realized that enabling Arimoto et al.'s invention to have available a

plurality of tests would allow for a more encompassing testing of the various DRAM memory cells and pages. This will benefit Arimoto et al.'s invention by giving the testing process the flexibility to perform a variety of tests so that the memory can be test for a variety of errors, which would not be possible with one testing procedure. It should be noted that Arimoto et al. explicitly mentions (column 17-18, lines 40-25) that this invention is not restricted to DRAM memory or does not have constraints on test patterns, hence it would have been obvious to one of ordinary skill in the art to incorporate a plurality if tests to allow for the testing of different types of memories. Further it should be noted that applying plurality of tests during parallel testing was commonly known method in the testing of memories at the time the invention was made and it would have been obvious to one of ordinary skill in the art to apply this in Arimoto et al.'s invention.

As per claim 11:

Arimoto et al. substantially teaches a tests enabler block reducing a number of pins required to test an integrated circuit, said tests enabler block (Figure 1, "TIC") being contained in said integrated circuit (Figure 1), said tests enabler block comprising: a first pin receiving a plurality of bits sequentially (Figure 1, "TD"), said plurality of bits forming a test code which indicates the specific one of test to be performed to test said integrated circuit (column 11, lines 1-40), wherein the plurality of bits indicates whether a test is to be performed (column 9, lines 1-50), further comprising a first storage element storing said plurality of bits (column 8, lines 40-42), wherein a bit value in each bit of said first storage element determines whether a test is to be performed (column 8,

lines 42-60, the "FIFO" is part of the "TIC", hence the FIFO indirectly determines whether a test is to be performed), further comprises a shift register into which said plurality of bits are shifted in sequentially after being received by said first pin (Figure 1 # 1), wherein said first storage element comprises a first register (Figure 1 # 10), wherein said plurality of bits are loaded from said shift register to said first register (column 8, lines 40-49).

Arimoto et al. does not explicitly teach performing a plurality of tests.

However Roohparvar in an analogous art teaches the method of parallel testing of memory cells performing a plurality of tests on the memory cells (column 5, lines 30-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the command decoder of Arimoto et al. to decode the plurality of bits into a plurality of tests after bit expansion, since one of ordinary skill in the art would have realized that enabling Arimoto et al.'s invention to have available a plurality of tests would allow for a more encompassing testing of the various DRAM memory cells and pages. This will benefit Arimoto et al.'s invention by giving the testing process the flexibility to perform a variety of tests so that the memory can be test for a variety of errors, which would not be possible with one testing procedure. It should be noted that Arimoto et al. explicitly mentions (column 17-18, lines 40-25) that this invention is not restricted to DRAM memory or does not have constraints on test patterns, hence it would have been obvious to one of ordinary skill in the art to incorporate a plurality if tests to allow for the testing of different types of memories. Further it should be noted that applying plurality of tests during parallel testing was

commonly known method in the testing of memories at the time the invention was made and it would have been obvious to one of ordinary skill in the art to apply this in Arimoto et al.'s invention.

As per claim 12:

Arimoto et al. substantially teaches a tests enabler block reducing a number of pins required to test an integrated circuit, said tests enabler block (Figure 1, "TIC") being contained in said integrated circuit (Figure 1), said tests enabler block comprising: a first pin receiving a plurality of bits sequentially (Figure 1, "TD"), said plurality of bits forming a test code which indicates the specific one of test to be performed to test said integrated circuit (column 11, lines 1-40), wherein the plurality of bits indicates whether a test is to be performed (column 9, lines 1-50), further comprising a first storage element storing said plurality of bits (column 8, lines 40-42), wherein a bit value in each bit of said first storage element determines whether a test is to be performed (column 8, lines 42-60, the "FIFO" is part of the "TIC", hence the FIFO indirectly determines whether a test is to be performed), further comprises a shift register into which said plurality of bits are shifted in sequentially after being received by said first pin (Figure 1 # 1), wherein said first storage element comprises a first register (Figure 1 # 10), wherein said plurality of bits are loaded from said shift register to said first register (column 8, lines 40-49), further comprises: a second pin receiving a status signal indicating whether said integrated circuit is to be operated in a test state or a functional state (Figure 1, "TCMD"); a phase pin receiving a phase signal (Figure 1, "TCLK"), wherein said phase signal operate said shift register in a shift phase in which said

plurality of bits are scanned into said shift register (columns 10-11, lines 65-5), and phase signals operate said first register in a load phase in which said plurality of bits are loaded from said shift register to said first register (Figure 1 # 3, column 8, lines 29-35, the CA shifter is indirectly controlled by the phase signals through the Latch/command decoder).

Arimoto et al. discloses the claimed invention except for having a plurality of phase pins and phase signals. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a plurality of phase pins and signals as opposed to one, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Arimoto et al. does not explicitly teach performing a plurality of tests.

However Roohparvar in an analogous art teaches the method of parallel testing of memory cells performing a plurality of tests on the memory cells (column 5, lines 30-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the command decoder of Arimoto et al. to decode the plurality of bits into a plurality of tests after bit expansion, since one of ordinary skill in the art would have realized that enabling Arimoto et al.'s invention to have available a plurality of tests would allow for a more encompassing testing of the various DRAM memory cells and pages. This will benefit Arimoto et al.'s invention by giving the testing process the flexibility to perform a variety of tests so that the memory can be test for a variety of errors, which would not be possible with one testing procedure. It should be

noted that Arimoto et al. explicitly mentions (column 17-18, lines 40-25) that this invention is not restricted to DRAM memory or does not have constraints on test patterns, hence it would have been obvious to one of ordinary skill in the art to incorporate a plurality if tests to allow for the testing of different types of memories. Further it should be noted that applying plurality of tests during parallel testing was commonly known method in the testing of memories at the time the invention was made and it would have been obvious to one of ordinary skill in the art to apply this in Arimoto et al.'s invention.

As per claim 13:

Arimoto et al. substantially teaches a tests enabler block reducing a number of pins required to test an integrated circuit, said tests enabler block (Figure 1, "TIC") being contained in said integrated circuit (Figure 1), said tests enabler block comprising: a first pin receiving a plurality of bits sequentially (Figure 1, "TD"), said plurality of bits forming a test code which indicates the specific one of test to be performed to test said integrated circuit (column 11, lines 1-40), wherein the plurality of bits indicates whether a test is to be performed (column 9, lines 1-50), further comprising a first storage element storing said plurality of bits (column 8, lines 40-42), wherein a bit value in each bit of said first storage element determines whether a test is to be performed (column 8, lines 42-60, the "FIFO" is part of the "TIC", hence the FIFO indirectly determines whether a test is to be performed), further comprises a shift register into which said plurality of bits are shifted in sequentially after being received by said first pin (Figure 1 # 1), wherein said first storage element comprises a first register (Figure 1 # 10),

wherein said plurality of bits are loaded from said shift register to said first register (column 8, lines 40-49), further comprises: a second pin receiving a status signal indicating whether said integrated circuit is to be operated in a test state or a functional state (Figure 1, "TCMD"); a phase pin receiving a phase signal (Figure 1, "TCLK"), wherein said phase signal operate said shift register in a shift phase in which said plurality of bits are scanned into said shift register (columns 10-11, lines 65-5), and phase signals operate said first register in a load phase in which said plurality of bits are loaded from said shift register to said first register (Figure 1 # 3, column 8, lines 29-35, the CA shifter is indirectly controlled by the phase signals through the Latch/command decoder).

Arimoto et al. discloses the claimed invention except for the invention to scan a new plurality of bits sequentially into said shift register while said plurality of tests being performed, wherein said new plurality of bits indicate a new plurality of tests to be performed. It would have been obvious to one having ordinary skill in the art at the time the invention was made to scan a new set of bits into the circuit through "TD", since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art. *In re Aller*,105 USPQ 233. wherein a new plurality of bits are scanned sequentially into said shift register while said plurality of tests being performed, wherein said new plurality of bits indicate a new plurality of tests to be performed.

Arimoto et al. discloses the claimed invention except for having a plurality of phase pins and phase signals. It would have been obvious to one having ordinary skill

in the art at the time the invention was made to use a plurality of phase pins and signals as opposed to one, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Arimoto et al. does not explicitly teach performing a plurality of tests.

However Roohparvar in an analogous art teaches the method of parallel testing of memory cells performing a plurality of tests on the memory cells (column 5, lines 30-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the command decoder of Arimoto et al. to decode the plurality of bits into a plurality of tests after bit expansion, since one of ordinary skill in the art would have realized that enabling Arimoto et al.'s invention to have available a plurality of tests would allow for a more encompassing testing of the various DRAM memory cells and pages. This will benefit Arimoto et al.'s invention by giving the testing process the flexibility to perform a variety of tests so that the memory can be test for a variety of errors, which would not be possible with one testing procedure. It should be noted that Arimoto et al. explicitly mentions (column 17-18, lines 40-25) that this invention is not restricted to DRAM memory or does not have constraints on test patterns, hence it would have been obvious to one of ordinary skill in the art to incorporate a plurality if tests to allow for the testing of different types of memories. Further it should be noted that applying plurality of tests during parallel testing was commonly known method in the testing of memories at the time the invention was made

and it would have been obvious to one of ordinary skill in the art to apply this in Arimoto et al.'s invention.

As per claim 14:

Arimoto et al. substantially teaches a tests enabler block reducing a number of pins required to test an integrated circuit, said tests enabler block (Figure 1, "TIC") being contained in said integrated circuit (Figure 1), said tests enabler block comprising: a first pin receiving a plurality of bits sequentially (Figure 1, "TD"), said plurality of bits forming a test code which indicates the specific one of test to be performed to test said integrated circuit (column 11, lines 1-40), wherein the plurality of bits indicates whether a test is to be performed (column 9, lines 1-50), further comprising a first storage element storing said plurality of bits (column 8, lines 40-42), wherein a bit value in each bit of said first storage element determines whether a test is to be performed (column 8, lines 42-60, the "FIFO" is part of the "TIC", hence the FIFO indirectly determines whether a test is to be performed), further comprises a shift register into which said plurality of bits are shifted in sequentially after being received by said first pin (Figure 1 # 1), wherein said first storage element comprises a first register (Figure 1 # 10), wherein said plurality of bits are loaded from said shift register to said first register (column 8, lines 40-49), further comprises: a second pin receiving a status signal indicating whether said integrated circuit is to be operated in a test state or a functional state (Figure 1, "TCMD"); a phase pin receiving a phase signal (Figure 1, "TCLK"), wherein said phase signal operate said shift register in a shift phase in which said plurality of bits are scanned into said shift register (columns 10-11, lines 65-5), and

phase signals operate said first register in a load phase in which said plurality of bits are loaded from said shift register to said first register (Figure 1 # 3, column 8, lines 29-35, the CA shifter is indirectly controlled by the phase signals through the Latch/command decoder). The tests enabler block of claim 13, wherein said scanning scans a plurality of control bits, said plurality of control bits representing control signals associated with said test (Figure 1 "TCMD").

Arimoto et al. discloses the claimed invention except for the invention to scan a new plurality of bits sequentially into said shift register while said plurality of tests being performed, wherein said new plurality of bits indicate a new plurality of tests to be performed. It would have been obvious to one having ordinary skill in the art at the time the invention was made to scan a new set of bits into the circuit through "TD", since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art. *In re Aller*, 105 USPQ 233 wherein a new plurality of bits are scanned sequentially into said shift register while said plurality of tests being performed, wherein said new plurality of bits indicate a new plurality of tests to be performed.

Arimoto et al. discloses the claimed invention except for having a plurality of phase pins and phase signals. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a plurality of phase pins and signals as opposed to one, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Arimoto et al. does not explicitly teach performing a plurality of tests, wherein said scanning scans a plurality of control bits on said pin.

However Roohparvar in an analogous art teaches the method of parallel testing of memory cells performing a plurality of tests on the memory cells (column 5, lines 30-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the command decoder of Arimoto et al. to decode the plurality of bits into a plurality of tests after bit expansion, since one of ordinary skill in the art would have realized that enabling Arimoto et al.'s invention to have available a plurality of tests would allow for a more encompassing testing of the various DRAM memory cells and pages. This will benefit Arimoto et al.'s invention by giving the testing process the flexibility to perform a variety of tests so that the memory can be test for a variety of errors, which would not be possible with one testing procedure. It should be noted that Arimoto et al. explicitly mentions (column 17-18, lines 40-25) that this invention is not restricted to DRAM memory or does not have constraints on test patterns, hence it would have been obvious to one of ordinary skill in the art to incorporate a plurality if tests to allow for the testing of different types of memories. Further it should be noted that applying plurality of tests during parallel testing was commonly known method in the testing of memories at the time the invention was made and it would have been obvious to one of ordinary skill in the art to apply this in Arimoto et al.'s invention. It would be obvious to one of ordinary skill in the art at the time the invention was made to scan the control bits (Figure 3, "TCMD") on the same pin as the data input pins since the bits are both being input into Figure 1 # 1, since one or

ordinary skill in the art would have realized that doing so would have allowed for further reducing the resources and hence making the testing more efficient. Further it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the same pin to input control bits and test input bits, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art. *In re Aller*,105 USPQ 233.

As per claim 15:

Arimoto et al. substantially teaches a tests enabler block reducing a number of pins required to test an integrated circuit, said tests enabler block (Figure 1, "TIC") being contained in said integrated circuit (Figure 1), said tests enabler block comprising: a first pin receiving a plurality of bits sequentially (Figure 1, "TD"), said plurality of bits forming a test code which indicates the specific one of test to be performed to test said integrated circuit (column 11, lines 1-40), wherein the plurality of bits indicates whether a test is to be performed (column 9, lines 1-50), further comprising a first storage element storing said plurality of bits (column 8, lines 40-42), wherein a bit value in each bit of said first storage element determines whether a test is to be performed (column 8, lines 42-60, the "FIFO" is part of the "TIC", hence the FIFO indirectly determines whether a test is to be performed), further comprises a shift register into which said plurality of bits are shifted in sequentially after being received by said first pin (Figure 1 # 1), wherein said first storage element comprises a first register (Figure 1 # 10), wherein said plurality of bits are loaded from said shift register to said first register

(column 8, lines 40-49), further comprises: a second pin receiving a status signal indicating whether said integrated circuit is to be operated in a test state or a functional state (Figure 1, "TCMD"); a phase pin receiving a phase signal (Figure 1, "TCLK"), wherein said phase signal operate said shift register in a shift phase in which said plurality of bits are scanned into said shift register (columns 10-11, lines 65-5), and phase signals operate said first register in a load phase in which said plurality of bits are loaded from said shift register to said first register (Figure 1 # 3, column 8, lines 29-35, the CA shifter is indirectly controlled by the phase signals through the Latch/command decoder). The tests enabler block of claim 13, wherein said scanning scans a plurality of control bits, said plurality of control bits representing control signals associated with said test (Figure 1 "TCMD"), wherein some bits of said test code are scanned in on a third pin (Figure 1, "TCLK") and some other bits of said test code are scanned in on a fourth pin (Figure 1, "TCMD"), wherein said first pin corresponds to one of said third pin and said fourth pin (columns 10-11, lines 60-15).

Arimoto et al. discloses the claimed invention except for the invention to scan a new plurality of bits sequentially into said shift register while said plurality of tests being performed, wherein said new plurality of bits indicate a new plurality of tests to be performed. It would have been obvious to one having ordinary skill in the art at the time the invention was made to scan a new set of bits into the circuit through "TD", since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art. *In re Aller*, 105 USPQ 233 wherein a new plurality of bits are scanned sequentially into said

shift register while said plurality of tests being performed, wherein said new plurality of bits indicate a new plurality of tests to be performed.

Arimoto et al. discloses the claimed invention except for having a plurality of phase pins and phase signals. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a plurality of phase pins and signals as opposed to one, since it has been held that mere duplication of the essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Arimoto et al. does not explicitly teach performing a plurality of tests, wherein said scanning scans a plurality of control bits on said pin.

However Roohparvar in an analogous art teaches the method of parallel testing of memory cells performing a plurality of tests on the memory cells (column 5, lines 30-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to allow the command decoder of Arimoto et al. to decode the plurality of bits into a plurality of tests after bit expansion, since one of ordinary skill in the art would have realized that enabling Arimoto et al.'s invention to have available a plurality of tests would allow for a more encompassing testing of the various DRAM memory cells and pages. This will benefit Arimoto et al.'s invention by giving the testing process the flexibility to perform a variety of tests so that the memory can be test for a variety of errors, which would not be possible with one testing procedure. It should be noted that Arimoto et al. explicitly mentions (column 17-18, lines 40-25) that this invention is not restricted to DRAM memory or does not have constraints on test

patterns, hence it would have been obvious to one of ordinary skill in the art to incorporate a plurality if tests to allow for the testing of different types of memories. Further it should be noted that applying plurality of tests during parallel testing was commonly known method in the testing of memories at the time the invention was made and it would have been obvious to one of ordinary skill in the art to apply this in Arimoto et al.'s invention. It would be obvious to one of ordinary skill in the art at the time the invention was made to scan the control bits (Figure 3, "TCMD") on the same pin as the data input pins since the bits are both being input into Figure 1 # 1, since one or ordinary skill in the art would have realized that doing so would have allowed for further reducing the resources and hence making the testing more efficient. Further it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the same pin to input control bits and test input bits, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable range involves only routine skill in the art. *In re Aller*,105 USPQ 233.

Related Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Additional pertinent prior arts, US Pat no. (4000460 A, 6800817 B2, 6438721 B1, 5224107 A), and US PG-Pub no. (20050240845 A1, 20030074615 A1) mention the same parallel testing procedure which includes scanning in a plurality of bits and using a shift register are included herein for Applicant's review.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to the final action is set to expire in THREE MONTH from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of the final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Saqib J. Siddiqui whose telephone number is (571) 272-6553. The examiner can normally be reached on 8:00 to 4:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free).

Saqib Siddiqui
Art Unit 2138
07/30/2006

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